Remarks/Arguments

Claims 1, 3-6, 8 and 9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Swenson (United States Patent No. 5,926,120) in view of Zaun (United States Patent Publication No. 2002/0024610). Applicant traverses these rejections for at least the following reasons.

The present invention provides a serial compressed bus interface, wherein received serial data is converted to packets of parallel data, and the packets of parallel data are transferred to an appropriate one of a plurality of devices associated with data applications in response to a signal from an enable logic.

In the exemplary embodiment, the serial data is received and converted to parallel data by serial to parallel converter 110. The parallel data is transferred to one of the buffers 130-136 in response to the buf_sel signal from enable logic 112. That is, the output of the enable logic 112 identifies which one of the buffers 130-136 is associated with a particular packet of parallel data output from serial to parallel converter 110. Such an arrangement advantageously reduces the pin count required in a serial interface, which receives time-division multiplexed serial data from a plurality of data sources and must transfer each respective data packet to an appropriate data application.

In that regard, Claim 1 recites:

> a serial-to-parallel converter having a single serial data input line adapted to receive time-division multiplexed serial data from a plurality of data sources, and having a plurality of parallel output lines for providing thereon a packet of said time-division multiplexed serial data in parallel form to one of a plurality of devices associated with data applications; and
>
> enable logic coupled to each of said plurality of devices and adapted to provide at least one data valid signal that identifies which of said plurality of devices is associated with a particular packet of said time-division multiplexed serial data.

The Swenson reference relates to a circuit for implementing a multi-channel parallel to serial conversion and a multi-channel serial to parallel conversion in one minimal RAM matrix. In that regard, Swenson shows in Fig. 1, registers 1-8 for receiving multi-channel serial data, RAM 10 for receiving the multi-channel serial data from the registers, MUX 11 for reading the data stored in RAM 10, and registers 21-28 for providing the data from RAM 10 to parallel form. In operation, serial data is received from registers 1-8 and stored in RAM 10 in accordance with address 9 until the matrix is full (col. 3, lines 24-46). MUX 11 reads the data from RAM 10 and provides the read data to each of registers 21-28 in accordance with address 9, applied to selector 12, in order to generate a block of parallel data (col. 3, lines 47-64).

The Examiner asserts that parts 21-28 correspond to the recited serial to parallel converter of Claim 1. However, a detailed review reveals this assertion is incorrect, as Claim 1 recites a serial-to-parallel converter having a single serial data input line adapted to receive time-division multiplexed serial data from a plurality of data sources, and having a plurality of parallel output lines for providing thereon a packet of said time-division multiplexed serial data in parallel form to one of a plurality of devices associated with data applications. (emphasis added)

Swenson shows registers 21-28 for providing serial to parallel output, but says nothing about providing the packet to one of a plurality of devices associated with data applications. In fact, the Office action is silent as to what portion of Swenson could even support teaching a plurality of devices associated with data applications. This is because no such passage or teaching exists. Swenson is directed to providing a multi-channel serial to parallel converter with a minimal number of elements, i.e., registers and RAM array. Swenson is not concerned with controlling the transfer of parallel data to other devices associated with data applications after it is output from the serial to parallel converter. Accordingly, there is no mention of any such devices or an enable logic that provides a data valid signal that

identifies which of the plurality of devices is associated with a particular packet of the time-division multiplexed serial data.

The above notwithstanding, the Examiner admits that Swenson fails to teach the recited enable logic. This further evidences Swenson is unconcerned with, and does not teach, providing the packet to one of a plurality of devices associated with data applications, as is recited by Claim 1.

In an attempt to remedy the shortcomings of Swenson to teach the recited enable logic of Claim 1, the Office action relies upon select teachings of Zaun. More particularly, the Office action relies upon par. [0020] of Zaun as teaching that IP control logic block 202 of Zaun equates to the recited enable logic of Claim 1, and may be properly combined with the system of Swenson to reach the recited invention of Claim 1. Applicant traverses this assertion.

Fig. 1 of Zaun illustrates a re-multiplexing module 100. *See, par. [0013].* Re-multiplexing module 100 includes an input processing system 102. *See, par. [0015].* Input processing system 102 includes an input processor 120. *See, par. [0016].* Fig. 2 of Zaun illustrates the components of input processor 120 – which the Office action referenced par. [0020] of Zaun dicusses. *See, par. [0018].*

Referring to FIG. 2 of Zaun, input data is sent to a serial-to-parallel converter 200, which converts the serial input stream from the input interface 118 to 8-bit parallel data. *See, par. [0019].* The converted data from the serial-to-parallel converter 200 is only sent to an input processor (IP) control logic block 202. *See, par. [0020].* Thus, serial to parallel converter 200, like the converter of Swenson, does not have a plurality of parallel output lines for providing thereon a packet of said time-division multiplexed serial data in parallel form <u>to one of a plurality of devices associated with data applications</u>.

Further, IP control block 202 merely sends received packets considered validated to the packet buffer 104 for storage. Thus, IP control block 202, like serial to parallel converter 200, merely provides the parallel data to a single device, and not to one of a plurality of devices associated with data applications – as is recited by Claim 1.

Accordingly, Zaun fails to remedy the herein-above discussed deficiencies of Swenson, such that a *prima facie* case of obviousness is lacking. Reconsideration and removal of this 35 U.S.C. 103 rejection is requested.

CONCLUSION

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. No fee is believed due in regard to the present amendment. However, if a fee is due, please charge the fee to Deposit Account 07-0832. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at 609-734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled.

Respectfully submitted,

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